REMARKS

1.) Claim Amendments

The Applicant has amended claims 1, 7, 13 and 21 and claims 8-12 have been canceled. Applicant respectfully submits no new matter has been added. Accordingly, claims 1-4 and 6-7 and 13-22 are pending in the application. Favorable reconsideration of the application is respectfully requested in view of the foregoing amendments and the following remarks.

2.) Claim Rejections – 35 U.S.C. § 103 (a)

Claims 1-4, and 6-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sauer (US 6,064,257) in view of Bezhad (US 6,759,904). Applicant has amended Claims 1, 7, 13 and 21 to overcome the rejections. Independent Claim 1 now claims the features of, *inter alia:*

> an amplifying means including the at least one oscillator amplifier and a corresponding at least one differential amplifier coupled to each of the at least one oscillator amplifier, wherein the amplifying means comprise P-Type MOS transistors;
>
> a load further comprising cascoded transistors coupled to the amplifying means and a power supply, wherein the cascoded transistors comprise P-Type Metal Oxide Semiconductor (MOS) transistors, the load being adapted to protect the amplifying means from interfering signals; and
>
> a tail current source coupled to the amplifying means, wherein the tail-current source comprise N-Type MOS transistors; wherein the width-over-length ratio of the transistors of the amplifying means is at least 3 times the width-over-length ratio of the transistors of the tail-current source and the width-over-length ratio of a second transistor pair of the load is at least 3 times the size of the width-over-length ratio of a first transistor pair of the load

As amended, the combination of Sauer and Bezhad fail to disclose, or suggest, the present invention. According to the Examiner, Sauer discloses:

> a device for generating a random sequence of bits, comprising; oscillating means [VCO/CCO 62] having an input terminal for receiving a bias as input, the oscillating means comprising at least one oscillator amplifier [017-030];
>
> amplifier means [015-030] comprising the at least one oscillator amplifier and a corresponding at least one differential amplifier [015 and 016] coupled to the at least one oscillator amplifier.
>
> The input bias terminal is coupled to a noise source [50] for generating intrinsic noise, the noise source comprising a noisy amplifier cell having amplifying means [G1-G4],
>
> a load [07-012] coupled to the amplifying means and supply, and a tail current source [11-14] coupled to grounding means and the amplifying means.

Applicant previously argued that while Sauer references the use of amplifiers, it does not disclose the use of cascoded transistors as the load as in the present invention. Applicant stated that Sauer fails to disclose a load further comprising cascoded transistors coupled to the amplifying means and a power supply, the load being adapted to protect the amplifying means from interfering signals.

The Examiner found Applicant's argument persuasive, but and now asserts Bezhad as supplying the missing features:

> Fig. 15 of Bezhad discloses a conventional differential common source, cascode amplifier, with transistors 1590 and 1592 cascoded with input transistors 1584 and 1586. He states that the amplifier further includes a tail current source [1588] and a common mode feedback circuit [1480].

The Examiner stated that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Sauer to utilize a conventional differential cascode amplifier, such as that disclosed by Bezhad, for the purpose of ensuring a higher slew rate output. Applicant now asserts that Bezhad fails to disclose the present invention as presently claimed. The description of Figure 15 of Bezhad is as follows:

Turning now to FIG. 15, there is depicted a simplified semi-schematic diagram of a nonlinear buffer, indicated generally at 1582, such as might be implemented as a wave shaping or squaring circuit 1352, 1354 or 1356 of FIG. 13. The nonlinear buffer 1582 receives a differential, sinusoidal input signal at the gate terminals of an input differential transistor pair 1584 and 1586. Drain terminals of the differential pair 1584 and 1586 are connected together in common and to a current sink supply 1588 which is coupled to a negative potential. Each of the differential pairs' respective source terminals are coupled to a bias network, including a pair of differential bias transistors 1590 and 1592 having their gate terminals tied together in common and coupled to a parallel connected bias network. The bias network is suitably constructed of a resistor 1594 and a current sink 1596 connected in series between a positive voltage potential such as Vdd and Vss. A bias node between 15 the resistor 1594 and current sink 1596 is coupled to the common gate terminals of the bias transistor network 1590 and 1592 and defines a bias voltage for the bias network which will be understood to be the positive supply value minus the IR drop across bias resistor 1594. The current promoting the IR drop across the bias resistor 1594 is, necessarily, the current I developed by the current sink 1596. A differential, square wave-type output (Vout) is developed at two output nodes disposed between the respective source terminals of the bias network transistors 1590 and 1592 and a respective pair of pull-up resistors 1598 and 1599 coupled, in turn, to the positive supply potential. It should be noted, that the bias network, including transistors 1590 and 1592, function to control the non-linear amplifier's common mode response in a manner similar to the linear amplifier's common mode network (transistors 1244 and 1246 and resistors 1248 and 1250 of FIG. 12). Although depicted and constructed so as to generate a differential square wave-type output in response to a differential sinusoidal input signal, the non-linear buffer 1582 of FIG. 15 is well suited for single-ended applications as well as for differential applications. If a single-ended output is desired, one need only take a signal from one of the two symmetric outputs. The choice of whether to implement the non-linear buffer as a single-ended or a differential buffer will depend solely on the input requirements of any follow on digital circuitry which the periodic signal generation circuit in accordance with the invention is intended to clock. This option is solely at the discretion of the system designer and has no particular bearing on practice of principles of the invention.

Applicant believes that the circuit elements of Bezhad are not properly equated to the MOS cascoded transistors used as a load in the present invention. First, the buffer depicted in Fig. 15 of Behzad is intended as a nonlinear buffer (See col. 26 line 2 through col. 27 line 46) making an input sinusoid a square wave at the output. In

particular the load comprises resistors (1598-99) and it is stated also in the text that they are "a pair of pull-up resistors" (col. 27 line 26).

Secondly, whereas the Examiner states that there is a common-mode feedback attached to the amplifier, presumably still referring to Fig. 15, however, the common-mode feedback is actually depicted in the amplifier shown seen in Fig. 14. The amplifier in Fig. 14 (described in columns 25-26) is an exemplary linear amplifier, more specifically, the folded cascode type where the input stage and the output load use the same polarity. While Behzad mentions cascode loads in this context (col. 26 line 37) the topology is significantly different than that of the present invention.

Third, to maximize the noise generated in the amplifier cells, it is generally desired to use small gate capacitors (i.e. small transistors), as described in the current application at page 16 line 33 and equations 2-4. In particular, equation 4 illustrates that the noise level is proportional to I_{ds}/L^2, where I_{ds} may be given by an over-all power consumption budget and will vary from one application to another. Given a certain I_{ds} budget, equation 4 dictates the minimize the channel length. Hence, the gate lengths are not merely design considerations nor can they be made arbitrarily short as a very small length will have a significant DC offset. This DC offset will manifest itself as a trend in the random number generation, that is generated ones will come to predominate over zeros.

Fourth, non-arbitrary mismatch considerations of the present invention are described in equations 5-9 in the present application, as claimed in amended claim 1. Equation 9 illustrates a need to make gate lengths short (to provide more noise) but also wide (to provide less mismatch). Equation 8 illustrates that the mismatch is optimized for V_{gs}-V_T is around 100mV, when the threshold and gain mismatches are roughly equal. Page 16, lines 5-16 discuss the reasons for not deviating from this optimum with the design recommendation discussed in lines 22-24.

Finally, Equation 10 illustrates the effect of the load, and specifically discusses that an inappropriate load will lower the gain (noise).

The above features of the present invention as claimed in Claim 1 are in stark contrast to normal design procedures where the gain-stage noise level is minimized rather than maximized (still subject to mismatch considerations). Normal design

procedures would result in much higher V_{gs} values as this would enhance linearity and improve matching, resulting in a higher slew rate (or smaller compensation capacitor due to a lower $gm/I_{ds}=2/(V^{gs}-V_T)$ ratio) and larger area to reduce noise (see equations 2+3b or 4).

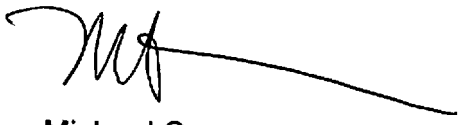
Hence, as illustrated, the teachings of Sauer and Bezhad are not sufficient to render the claims obvious (See *In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)*). In re Ratti, the court reversed the rejection of a patent application holding the "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which the [primary reference] construction was designed to operate." 270 F.2d at 813, 123 USPQ at 352.

CONCLUSION

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant, therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for all pending claims.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted,



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